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High dielectric constant materials and their application to IC gate stack systems

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Abstract: High dielectric constant (high-k) materials are vital to the nanoelectronic devices. The paper reviews research development of high-k materials, describes a variety of manufacture technologies and discusses the application of the gate stack systems to non-classical device structures.

Key words: dielectric constant; gate stack; alternative materials

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1 Introduction

Silicon dioxide (SiO_2) has long been the key gate dielectric material exhibiting superior electrical isolation property and stable, high quality Si-SiO_2 interface. However, for nanoelectronic technology the alternative gate dielectric materials have to be found to replace SiO_2. The candidate materials are required the systematic properties such as: permittivity, band gap, thermodynamic stability, interface quality, film morphology, process compatibility and reliability. These new materials will be the major issue for nanoelectronic era, in particular, for the semiconductor IC technology nodes below 45 nm, which will strongly focus on three-dimensional transistor architecture. One of the new device architectures, being increasingly known as "finFET", is essentially wrapped around by high-k gate dielectrics. In the current version of the ITRS, the scaling of the MOSFET is followed to the year 2016 when the channel length should be 9 nm. In general, as devices are scaled to smallest dimensions, the physical behavior of the system at the atomic level becomes more important to a description of device function. Not only a fundamental research, in view of transistor function, needs to be developed but also the semiconductor community ought to search for new alternative materials.

2 Basic concepts

The band diagram for SiO_2 gate oxide is shown in Fig. 1 where the features include a large offset between the conduction and valence bands of the oxide and the silicon. These offsets serve as a barrier to electron or hole conduction across the oxide and limit leakage current. The dielectric displacement is continuous

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across the interface provided interface charges or traps are absent at the interface. Such traps and charges mitigate the field from the oxide penetrating into the silicon. These features (see Fig. 1) of the band diagram are critical to the function of the transistor.

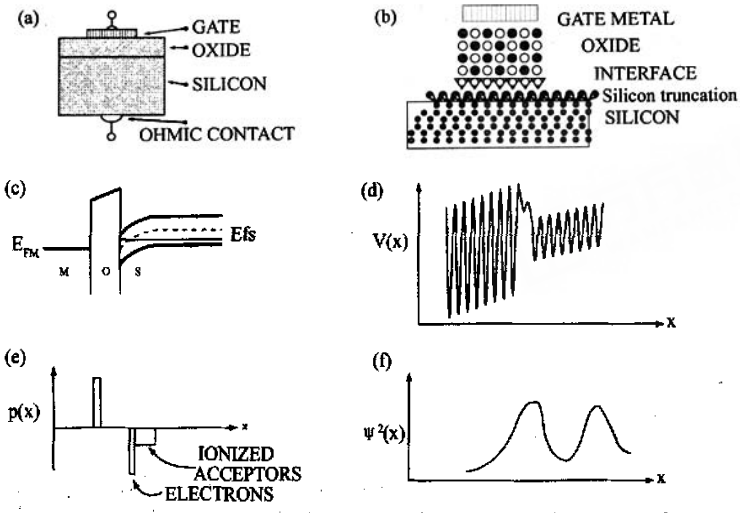

Fig. 1 Comparison between the classical view and the atomic-layer view of a MOS capacitor

Major scaling changes were implemented in the reduction of the gate dielectric thickness, physical gate length and extension junction depth, which have been discussed by Dennard *et al.*[1]. As the gate oxide thickness shrinks to less than 3 nm , quantum mechanical effects on the electrical structure and transport properties will become evident. For thin oxides and high-k dielectric, the capacitance voltage (CV) curve shows all anomalous decrease of capacitance in accumulation[2]. The reason is that the electron density in the silicon at the oxide-silicon interface is reduced due to quantum mechanical confinement. To correct for this effect, it is modeled by assuming that the electron wave function is zero at the interface[3]. The fact that the wave function non-zero in the oxide has been used as a correction for leakage current calculations due to quantum mechanical tunneling[4,5]. These properties are sensitive to the band offsets of the oxide-silicon stack. In addition, the equivalent oxide thickness (EOT) is a useful value to select the high-k material which can meet the requirement for specific device. Researchers at IMEC in Belgium, for example, are aiming to achieve EOT values of 0.5—1.2 nm for high-speed, high-performance devices and EOT values of 1.2—1.6 nm for low standby power logic applications.

International Technology Roadmap for Semiconductors 2004 Update (ITRS 2004 Update) highlights high-k materials and points out that there is a growing consensus that both high-k and metal gates are likely to be introduced simultaneously, rather than suggested. It has been emphasized that introduction and process integration of high-k gate stack materials and processes are needed for high performance, low operating and low standby power MOSFETs. It is also the key issues that removal of high-k dielectric without loss of the underlying silicon and metrology and characterization associated with gate dielectric film thickness and gate stack electronic properties.

3 Investigation on alternative materials

The high-k materials which had been investigated at the initial stage were Ta_2O_5, $SrTiO_3$ and

Al_2O_3[6]. Recently Lee[7] and Klie[8] have studied other metal oxides. Campbell[9], Yamamichi[10], Wilk[11-13] and Oston[14] suggested the rare earth oxides such as CeO_2, Pr_2O_3, PrO_2, Y_2O_3, La_2O_3 as the potential candidate high-k materials for the next generation IC.

The non-crystalline high-k materials are, according to the morphologies, classified into three groups which are: (1) continuous random networks (CRN), (2) modified continuous random networks (MCRN), (3) random close packed (RCP) non-periodic solids. Their physical properties are listed in Table 1.

Table 1 Some physical properties

Dielectric	ΔX	I_b	coordination	coordination
CNRS			Metal/silicon	oxygen
SiO_2	1.54	0.45	4	2.0
MCRNS				
Al_2O_3	1.84	0.57	4 and 6 (3∶1)	3.0
Ta_2O_5	1.94	0.61	6 and 8 (1∶1)	2.8
TiO_2	1.90	0.59	6	3.0
$(ZrO_2)_{0.1}(SiO_2)_{0.9}$	1.61	0.48	8 and 4	2.2
$(ZrO_2)_{0.23}(SiO_2)_{0.77}$	1.70	0.51	8 and 4	2.46
$(ZrO_2)_{0.5}(SiO_2)_{0.5}$	1.88	0.59	8 and 4	3.0
$(TiO_2)_{0.5}(SiO_2)_{0.5}$	1.72	0.52	6 and 4	2.5
$(Y_2O_3)_1(SiO_2)_2$	1.88	0.59	8 and 4	2.86
$(Y_2O_3)_2(SiO_2)_3$	1.93	0.61	8 and 4	3.0
$(Y_2O_3)_1(SiO_2)_1$	1.99	0.63	8 and 4	3.11
$(Al_2O_3)_4(ZrO_2)_1$	2.02	0.64	8 and 4	3.0
$(Al_2O_3)_3(Y_2O_3)_1$	1.97	0.62	8 and 4	3.0
RANDOM IONS				
HfO_2	2.14	0.68	8	4.0
ZrO_2	2.22	0.71	8	4.0
$(La_2O_3)_2(SiO_2)_1$	2.18	0.70	6 and 4	3.5
Y_2O_3	2.2	0.7	6	4.0
La_2O_3	2.34	0.75	6	4.0

Note: ΔX — Electronegativity difference; I_b — Average bond ionicity

The ab initio calculation has also been applied to search high-k materials based on relatively small clusters with at least two shells of the near neighbor[15-17]. The preliminary results of HfO_2 and TiO_2 based on ab initio calculation yield good agreement with experiment. These calculations are being extended to complex oxides, which ensure that electronic states of these atoms can coupled through bonding to the same O-atom as in $GdSeO_3$, $HfTiO_4$ and $LaLuO_3$.

McKee *et al.*[18] solved the problems of growing crystalline oxide on silicon (COS). Crystalline dielectrics may hold advantages over high-k amorphous films for they have higher dielectric constants, higher quality interfaces and lower defect densities. $SrTiO_3$ and $BaTiO_3$ have been chosen as the candidates for crystalline oxides. Alkaline earth oxides have been thoroughly studied[19-23].

4 Development of manufacturing methods

The transition to the high-k materials represents a fundamental change in chemical processing towards deposited dielectrics and away from dielectrics that can be thermally grown on crystalline silicon. To ensure

good electrical performance of the resulting devices, the deposited dielectrics must have an excellent thickness uniformity and superior interfacial and bulk properties. The following techniques are currently employed: (1) Atomic layer deposition (ALD); (2) Chemical vapor deposition (CVD); (3) Pulsed laser deposition (PLD); (4) Sol-gel deposition; (5) Sputtering; (6) Ion beam assisted deposition (IBAD); (7) Molecular beam epitaxy (MBE); (8) Plasma enhanced CVD (PECVD); (9) Plasma enhanced ALD (PEALD).

(1) ALD is referred to the binary chemical reaction and has two major features: the deposition consisting a sequence of self-limiting process steps; each self-limiting step leading to a monolayer saturation. Fig. 2 illustrates the configuration of the ALD equipment.

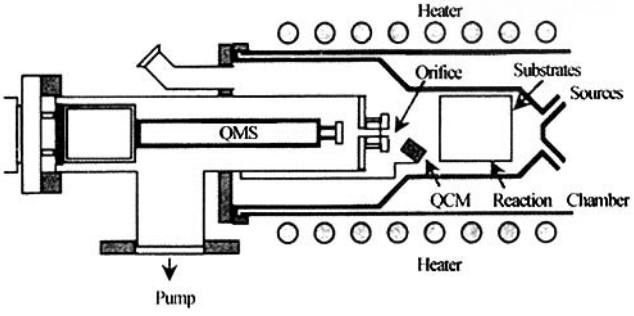

Fig. 2 Configuration of the ALD equipment

(2) CVD is widely employed in manufacturing the thin films. For CVD of high-k materials, the metal-containing precursors with or without the oxidizing agents are directed to a heated surface leading to their decomposition and the deposition of high-k materials. Metal halides are avoided in CVD processes due to their higher deposition temperatures, and oxygen is normally used as the oxidant. CVD reactor geometry and temperature gradient can affect the follow structures, deposition rates and composition uniformity.

(3) PLD is a laser ablation method to deposit high-k materials. Disbiens *et al.*[24] employed a KrF laser with energy density of 2—3 J/cm^2 at 248 nm wavelength and a Ti-Si target to fabricate titanium silicate thin films. The laser is usually pulsed at 30—60 Hz for 10—20 ns and ablates a metal target.

(4) Sol-gel deposition is a wet chemical process. Reaction of metal halides and alkoxides forms metal oxides and alkyl halides under the non-hydrolytic conditions. High-k materials such as zirconium oxide have been deposited by sol-gel processing.

(5) Sputtering: Reactive sputtering deposition and metal sputtering deposition are frequently used for manufacturing high-k materials. The reactive sputtering deposition can either use a metal oxide target being bombarded by an inert plasma or use a metal target being bombarded by an oxidizing discharge[25—27].

(6) IBAD generates energetic ions to accelerate the surface reaction of precursor atoms deposited on a substrate. IBAD is a vital technique for preparing high-k materials, where the ion bombardment is the key factor controlling thin film properties and complex metal oxides can be deposited without the use of many chemical precursors.

(7) MBE: Metal oxide thin films such as Al_2O_3, Y_2O_3 and $SrTiO_3$ can be deposited by MBE using molecular oxygen and thermally evaporated metals. They are crystalline, stoichiometric and atomically smooth. Most MBE deposited high-k films have very low leakage current and interface state densities. Very high dielectric constants have also been observed for crystalline perovskite oxides by MBE.

(8) PECVD: High-k materials, the meta-containing precursor and molecular oxygen are dissociated and ionized in the gas phase in PECVD processes. The reaction is to generate the metal oxide precursor deposi-

ted on the surface to form high-k metal oxides. This ion and radical assisted deposition can occur at near room temperature. Thus PECVD processing both has the high deposition rate and the flexibility of controlling the film deposition and morphology.

(9) PEALD has been effectively used to prepare high-k thin films[28,29], which has two advantages of the increased reaction rate and an improved removal of volatile products at lower temperatures since the radicals can react with the surface ligands with minimal to no activation energy barrier.

5 Application to the gate stack system

Fig. 3 summarizes the tunneling currents through different dielectrics and it illustrates the tunneling current decreases with increasing dielectric constant i. e. , with increasing physical thickness. However, the drain leakage current will increase with increasing the physical thickness for drain electric fields couple through the gate dielectric to the source-channel junction, and lowers the potential barrier. Hence the compromised dielectrics must be chosen to minimize the gate leakage current as well as the drain leakage current. In addition, since some residual oxide normally exists on the silicon substrate the tunneling current through the gate stacks is higher than that through the pure dielectrics due to the reduced thickness.

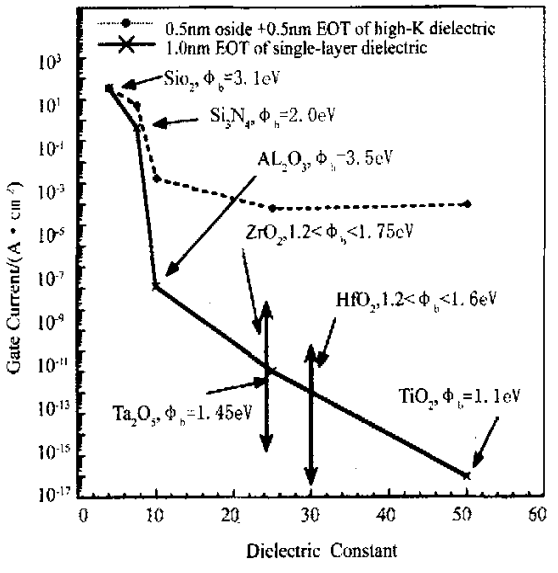

Fig. 3 Tunneling currents through different dielectrics

Hobbs[30], Lee[31] and Lent *et al.*[32] investigated ZrO_2 and HfO_2 for transistor applications. Fan, *et al.*[33] conducted the experiment and simulation from the same device structure. The device structural information of ZrO_2 and HfO_2 MOSCAP has been obtained from Cg-Vg and Ig-Vg simulation, which was in good agreement with experimental results for different thickness of gate dielectric stack.

The electrical reliability of those new gate dielectrics must also be considered critical for application in CMOS technology. Wallace *et al.*[34] emphasized the importance of investigating the characteristics of the alternative dielectric materials connected with devices, which may exhibit subtleties in reliability.

6 Conclusion

The evolution of the conventional MOS to non-classical MOS devices and the transition to nanometric technology nodes of IC require high-k gate dielectrics. Research efforts have been described in developing

the new materials systems which have suitable permittivity, barrier height, thermal stability; and good interface quality, film morphology, process compatibility and reliability. Manufacturing methods and application to the MOS device gate stack systems have been also discussed.

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